1. Polling takes more time than interrupts. However, if we know that certain even will last certain amount of time, polling can be ideal.

4.

(a) ISR first.

(b) ISR first.

(c) CPU first.

(d) CPU first.

5.

(a) Software context save and restore is performed.

(b) Shadow register set reduces ISR entry and exit time

8.

(a)

IEC0SET = 0b1<<8; // enable the 8th bit

IFS0CLR = 0b1<<8;

IPC2CLR = 0x001F;

IPC2SET = 0b00010110;

(b)

IEC1SET = 0b1<<15;

IFS1CLR = 0b1<<15;

IPC8CLR = 0x1F<<24;

IPC8SET = 0b11001<<24;

(c)

IEC2SET = 0b1<<4;

IFS2CLR = 0b1<<4;

IPC12CLR = 0x1F<<8;

IPC12SET = 0b11111<<8;

(d)

IEC0SET = 0b1<<11;

IFS0CLR = 0b1<<11;

IPC2CLR = 0x1F<<24;

IPC2SET = 0b1110<<8;

INCONSET = 1;

3.

(a) Float and long double have jumps.

Text

Description automatically generated with medium confidence

(b) Char, int, long long int do not have jumps. Char is not involved in the smallest data type. Char has an extra andi command which will remove the most significant bit.

(c)

Table

Description automatically generated

(d)

According to the screenshot, subadd is one of the subroutines that uses0x430 bytes of memory.

Graphical user interface

Description automatically generated with medium confidence

4.

Table

Description automatically generated with low confidence